What is claimed is:

1. A command input circuit comprising:

a clock signal supplying unit which supplies a clock signal to a first command acquisition unit and a second command acquisition unit;

a command input unit which receives a first command and a second command, and supplies the first command and the second command to a first command acquisition unit and a second command acquisition unit;

said first command acquisition unit which acquires said first command in response to a first edge of said clock signal, where the first edge is one of a rising edge and a falling edge of the clock signal; and

said second command acquisition unit which acquires said second command in response to a second edge of said clock signal, where the second edge is an edge of the clock signal which is different from said first edge.

2. A data handling device comprising:

a clock signal supplying unit which supplies a clock signal to a first command acquisition unit and a second command acquisition unit;

a command input unit which receives a first command and a second command, and supplies the first command and the second command to a first command acquisition unit and a second command acquisition unit;

said first command acquisition unit which acquires said first command in response to a first edge of said clock signal, where the first edge is one of a rising edge and a falling edge of the clock signal;

said second command acquisition unit which acquires said second command in response to a second edge of said clock signal, where the second edge is an edge of the clock signal which is different from said first edge; and

a processing unit which performs processing in accordance with said first command and said second command.

3. The data handling device according to claim 2, wherein said processing unit starts said processing when the processing unit receives said first command.

4. The data handling device according to claim 3, wherein said processing unit stops said processing when said processing unit determines that said second command is not normal.

5. The data handling device according to claim 3, wherein said processing unit goes into a predetermined operation mode corresponding to said second command when the processing unit receives the second command.

6. The data handling device according to claim 2,

further comprising,

an address input unit which receives a first address and a second address, and supplies the first address and the second address to a first address acquisition unit and a second address acquisition unit,

said first address acquisition unit which acquires said first address in response to said first edge of said clock signal, and

said second address acquisition unit which acquires said second address in response to said second edge of said clock signal.

7. The data handling device according to claim 2, further comprising a data input-and-output unit which receives and outputs data in response to said rising edge and said falling edge of the clock signal.

8. A command input circuit comprising:

m command acquisition units which are provided corresponding to first to mth commands, respectively, where m is an integer greater than one;

a clock signal supplying unit which supplies n clock signals respectively having different phases to said m command acquisition units, where n is an integer greater than one; and

a command input unit which receives said first to mth commands, and supplies the first to mth commands to

said m command acquisition units;

wherein each of the m command acquisition units acquires one of said first to mth commands corresponding to said each of the m command acquisition units in response to one of m edges of said n clock signals corresponding to said one of the first to mth commands.

9. A data handling device comprising:

m command acquisition units which are provided corresponding to first to mth commands, respectively, where m is an integer greater than one;

a clock signal supplying unit which supplies n clock signals respectively having different phases to said m command acquisition units, where n is an integer greater than one;

a command input unit which receives said first to mth commands, and supplies the first to mth commands to said m command acquisition units; and

a processing unit which performs processing in accordance with said first to mth commands;

wherein each of the m command acquisition units acquires one of said first to mth commands corresponding to said each of the m command acquisition units in response to one of m edges of said n clock signals corresponding to said one of the first to mth commands.

10. The data handling device according to claim 9,

wherein said processing unit starts said processing when the processing unit receives said first command.

11. The data handling device according to claim 10, wherein said processing unit stops said processing when said processing unit determines that one of said second to mth commands is not normal.

12. The data handling device according to claim 10, wherein said processing unit goes into a predetermined operation mode corresponding to one of said second to mth commands when the processing unit receives said one of said second to mth commands.

13. The data handling device according to claim 9, wherein said first command indicates one of no operation, a read operation, and a write operation,

said processing unit starts said processing when the processing unit receives said first command, and

when the processing unit receives at least a portion of said second to mth commands, said processing unit determines whether to continue one of said read operation and said write operation or to go into a predetermined operation mode, according to a combination of the first command and said at least a portion of said second to mth commands.

14. The data handling device according to claim 9, further comprising,

first to pth address acquisition units which are provided corresponding to first to pth addresses, respectively, where p is an integer greater than one, and

an address input unit which receives said first to pth addresses, and supplies the first to pth addresses to said first to pth address acquisition units,

wherein each of said first to pth address acquisition units acquires one of said first to pth addresses corresponding to said each of said first to pth address acquisition units in response to one of first to pth edges of said n clock signals corresponding to said one of the first to pth addresses.

15. The data handling device according to claim 9, further comprising a data input-and-output unit which receives or outputs data in response to j edges of the n clock signals, where j is an integer greater than one.